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# Voltage Reference Design Considerations for a High Performance System

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# Introduction

- Selection of Voltage Reference
- Improvement in the performance!
- Component Selection & Layout
- How to test?

# Voltage Reference Selection

- The ADC noise budget is dominated by Voltage Reference noise as referred to ADC input
- voltage reference stability and noise define measurement limits in instrumentation systems.
- The Choice of Reference Voltage is decide by the ADC
- On Chip Reference?
  - On same die as that of digital and Analog switching sections
  - ADC chip has speed dependent power loss
  - Susceptible to noise and temperature drift

# ADC Specifications

**AC SPECIFICATIONS, $V_{REF}$ = 1.0 V**

AVDD = 1.8 V, DRVDD = 1.8 V, 2.0 V p-p full-scale differential input, 1.0 V reference, $A_{IN}$ = −1.0 dBFS, unless otherwise noted.

Table 4.

| Parameter[1] | Temperature | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SIGNAL-TO-NOISE RATIO (SNR) | | | | | |
| $f_{IN}$ = 9.7 MHz | 25°C | | 78 | | dBFS |
| $f_{IN}$ = 16 MHz | 25°C | | 77.9 | | dBFS |
| $f_{IN}$ = 64 MHz | 25°C | | 76.8 | | dBFS |
| $f_{IN}$ = 128 MHz | 25°C | | 74.3 | | dBFS |
| $f_{IN}$ = 201 MHz | 25°C | | 72.1 | | dBFS |
| $f_{IN}$ = 301 MHz | 25°C | | 69.3 | | dBFS |

**AC SPECIFICATIONS, $V_{REF}$ = 1.4 V**

AVDD = 1.8 V, DRVDD = 1.8 V, 2.8 V p-p full-scale differential input, 1.4 V reference, $A_{IN}$ = −1.0 dBFS, unless otherwise noted.

Table 3.

| Parameter[1] | Temperature | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SIGNAL-TO-NOISE RATIO (SNR) | | | | | |
| $f_{IN}$ = 9.7 MHz | 25°C | | 80.1 | | dBFS |
| $f_{IN}$ = 16 MHz | 25°C | | 79.9 | | dBFS |
| $f_{IN}$ = 64 MHz | 25°C | 75.7 | 78.1 | | dBFS |
| $f_{IN}$ = 128 MHz | 25°C | | 75 | | dBFS |
| $f_{IN}$ = 201 MHz | 25°C | | 72.7 | | dBFS |
| $f_{IN}$ = 301 MHz | 25°C | | 69.7 | | dBFS |

AD9656 has 2dB additional SNR at 16MHz

# Voltage Reference Specifications

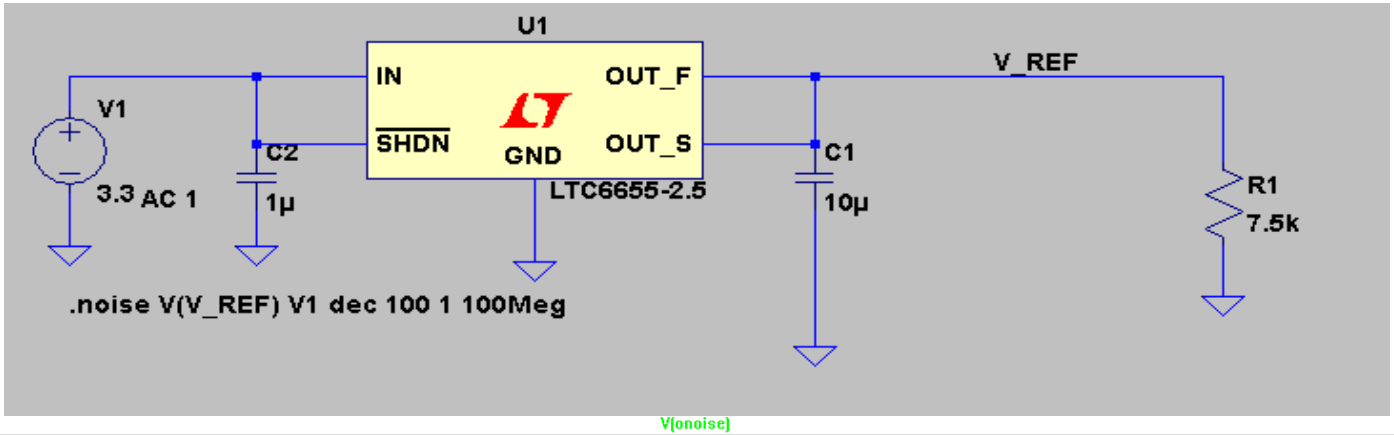
High accuracy
Low noise
Current drive capacity
Good load regulation
Low thermal drift
Low Long term drift
Low environment sensitivity
Low dropout voltage
1.4V is a non standard value

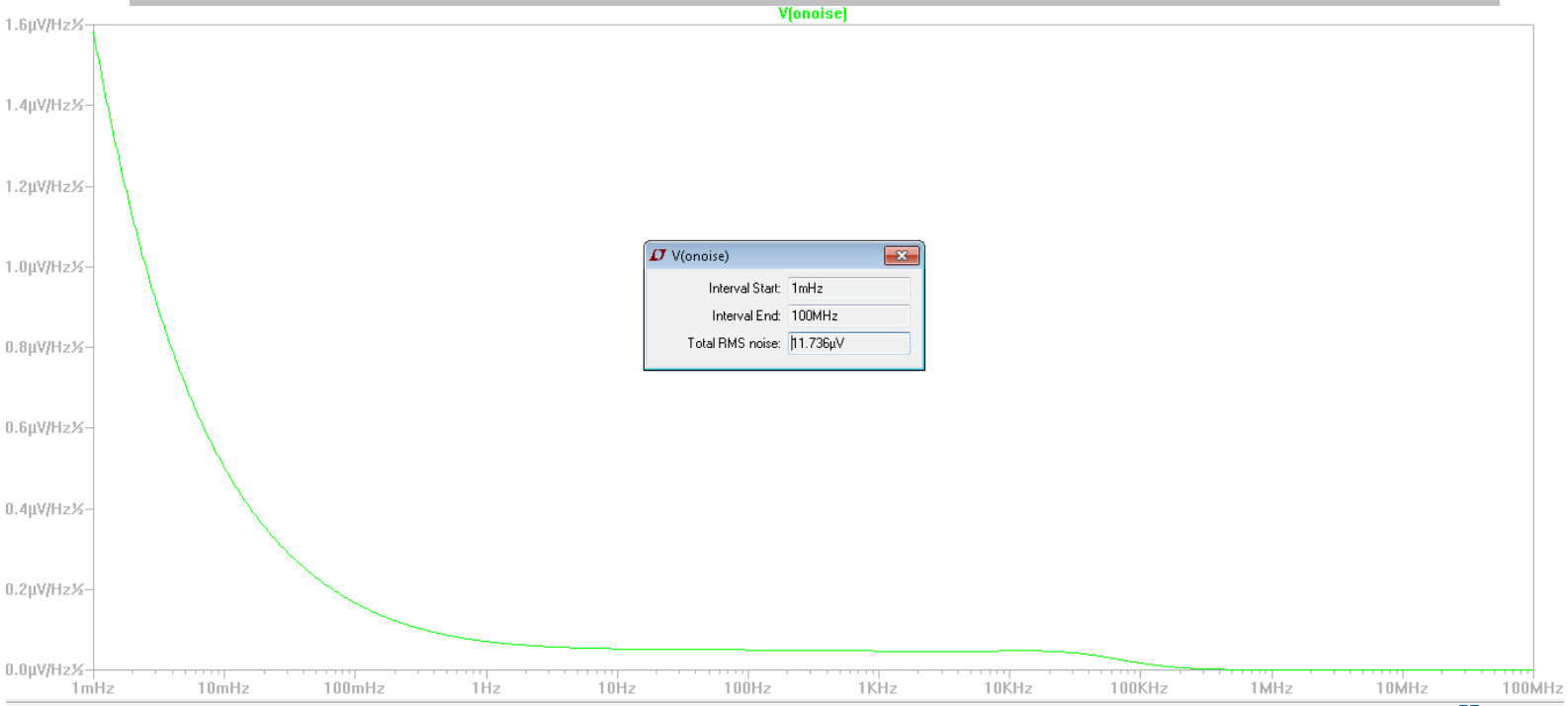
## LTC 6655-2.5

### FEATURES

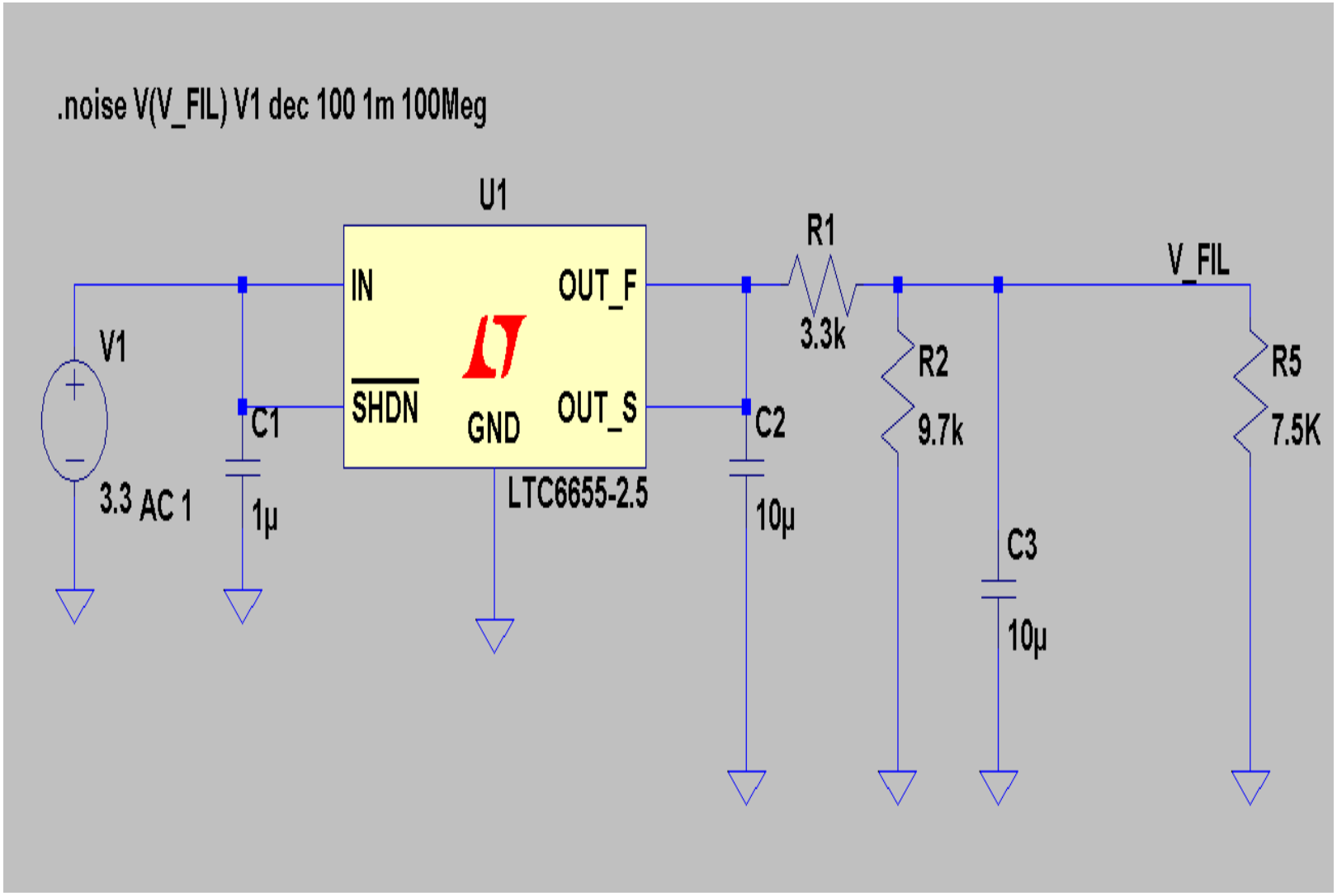
- Low Noise: 0.25ppm$_{P-P}$ (0.1Hz to 10Hz)
  625nV$_{P-P}$ for the LTC6655-2.5
- Low Drift: 2ppm/°C Max
- High Accuracy: ±0.025% Max
- No Humidity Sensitivity (LS8 Package)
- Thermal Hysteresis (LS8): 30ppm (–40°C to 85°C)
- Long-Term Drift (LS8): 20ppm/$\sqrt{kHr}$
- 100% Tested at –40°C, 25°C and 125°C
- Load Regulation: <10ppm/mA
- Sinks and Sources Current: ±5mA
- Low Dropout: 500mV
- Maximum Supply Voltage: 13.2V
- Low Power Shutdown: <20µA Max
- Available Output Voltages: 1.25V, 2.048V, 2.5V, 3V, 3.3V, 4.096V, 5V
- Available in an 8-Lead MSOP and High Stability Hermetic 5mm × 5mm LS8 Packages

# Noise performance

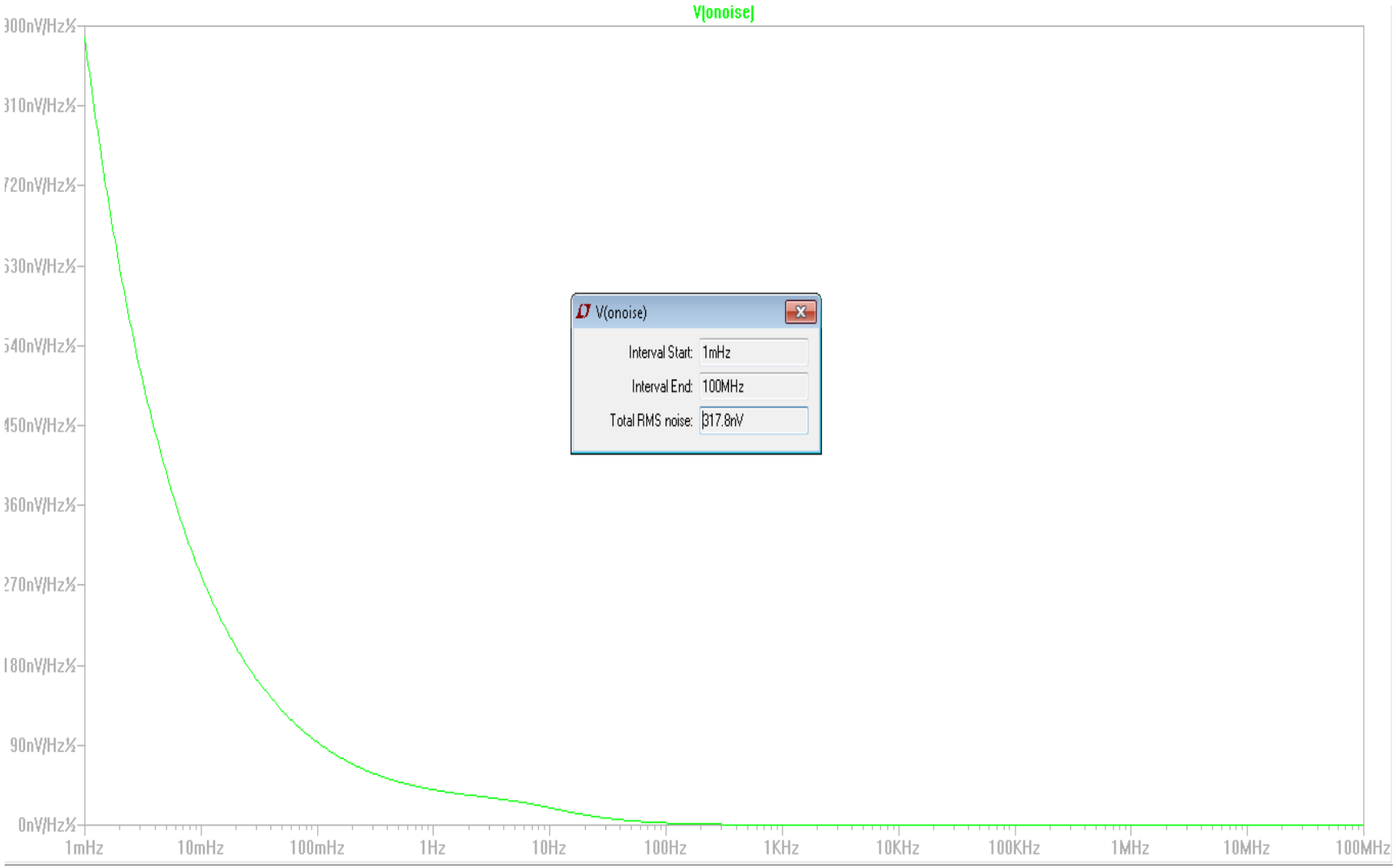


# Can we Improve It?



# Can we Improve It?

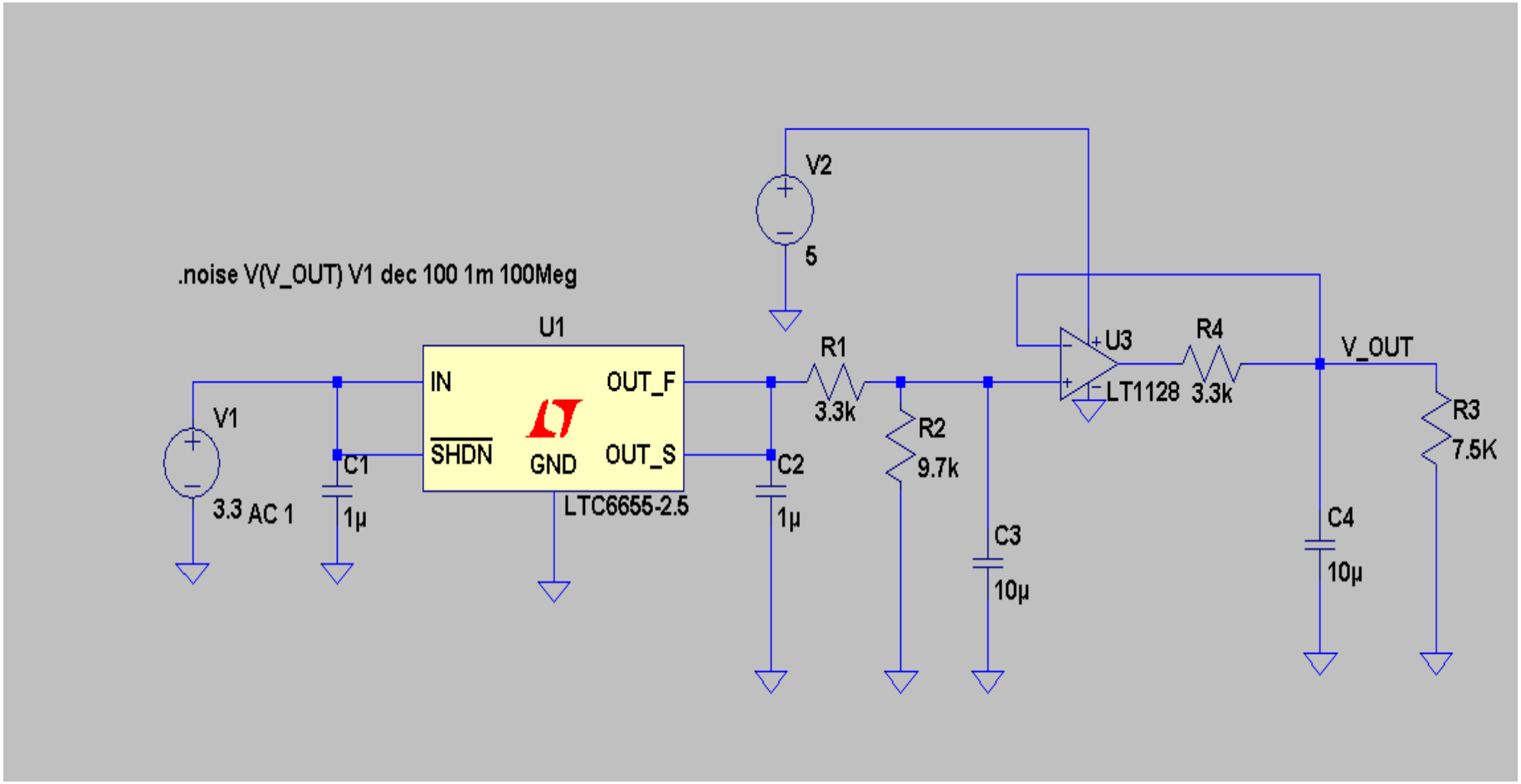


# What about ADC Reference Resistor

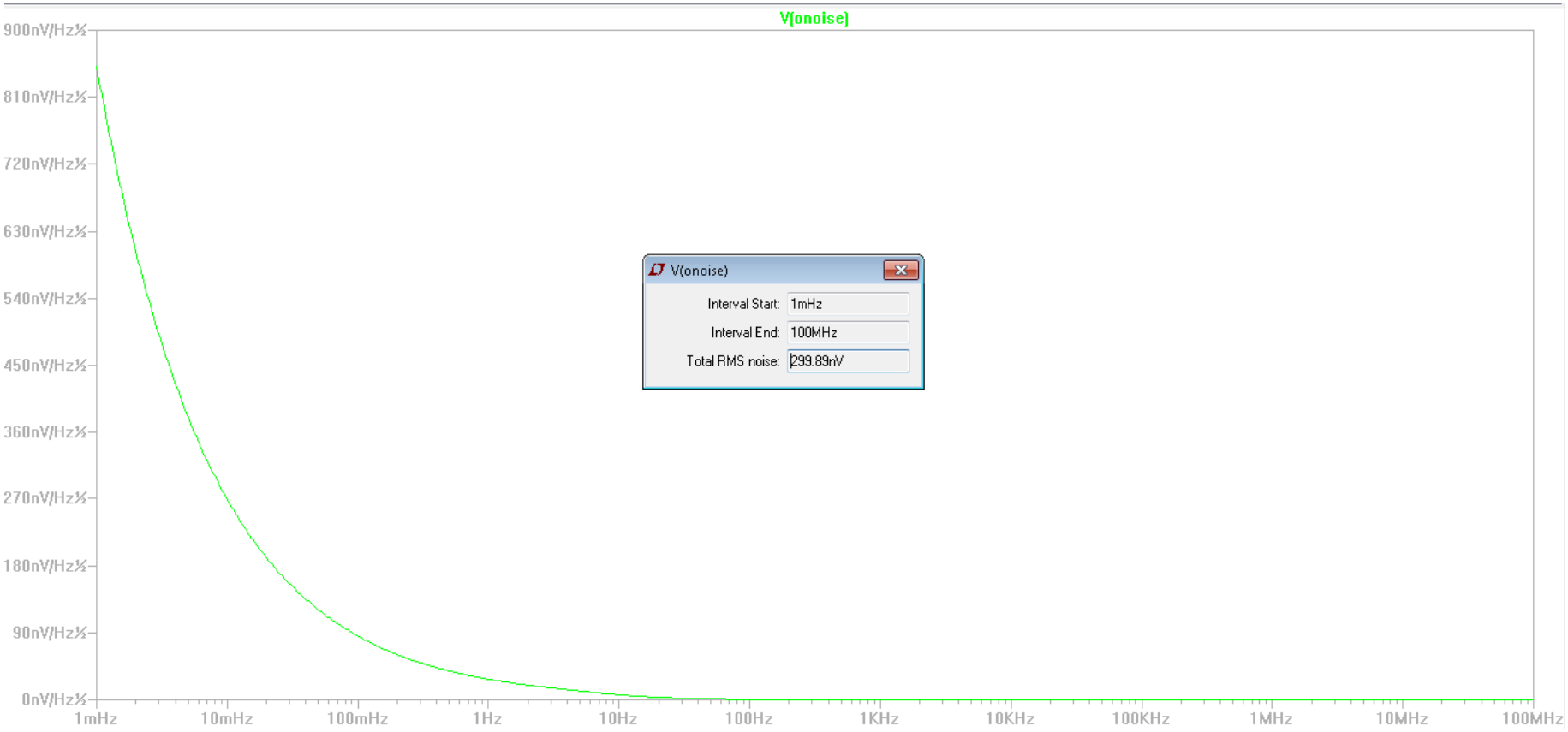
- ADC internal Impedance is deciding the voltage
- ADC internal Impedance is temperature dependent
- It can very as much as 10% with temperature and varies from device to device
- Multiple ADC will disturb the Reference voltage
- Voltage reference output impedance is high

| | | | | | |
|---|---|---|---|---|---|
| Offset Error | Full | | 2 | | ppm/°C |
| INTERNAL VOLTAGE REFERENCE | | | | | |
| Output Voltage | 25°C | 1.37 | 1.4 | 1.41 | V |
| Load Regulation at 1.0 mA | 25°C | | 4 | | mV |
| Input Resistance | 25°C | | 7.5 | | kΩ |
| INPUT-REFERRED NOISE | | | | | |
| $V_{REF}$ = 1.4 V | 25°C | | 2.1 | | LSB rms |
| ANALOG INPUTS | | | | | |

# Low Noise Buffered output



# Low Noise Buffered output



# Layout and component selection

- Never use ceramic capacitors. On even on power supply lines of ADC and Reference. They generate micro-phonics. Use NP0 capacitors
- Use an LDO to power the reference chip
- Keep a continuous ground plane below the chip for noise isolation and thermal heat removal
- Place reference section close to ADC
- Shield the Reference output lines

# Testing of Reference

- The Key specification of testing is
  - Reference 1/f noise
  - Reference white noise
  - Reference RMS noise
  - Reference drift with time
  - Reference transient load response

- 1/f noise measurement needs special kind of testing unit
  - The measuring instrument 1/f performance will dominate the results.

# Measurement unit

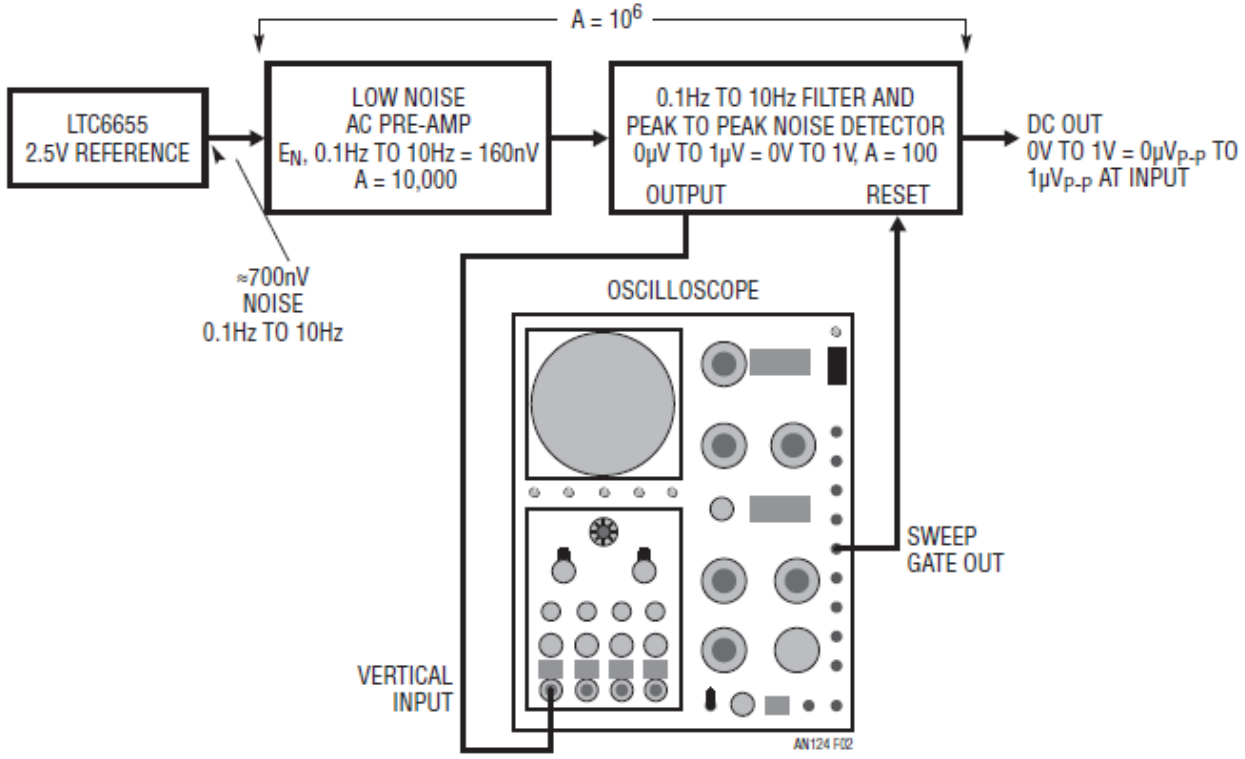



**Figure 2. Conceptual 0.1Hz to 10Hz Noise Testing Scheme Includes Low Noise Pre-Amplifier, Filter and Peak to Peak Noise Detector. Pre-Amplifier's 160nV Noise Floor, Enabling Accurate Measurement, Requires Special Design and Layout Techniques**

# Measurement unit

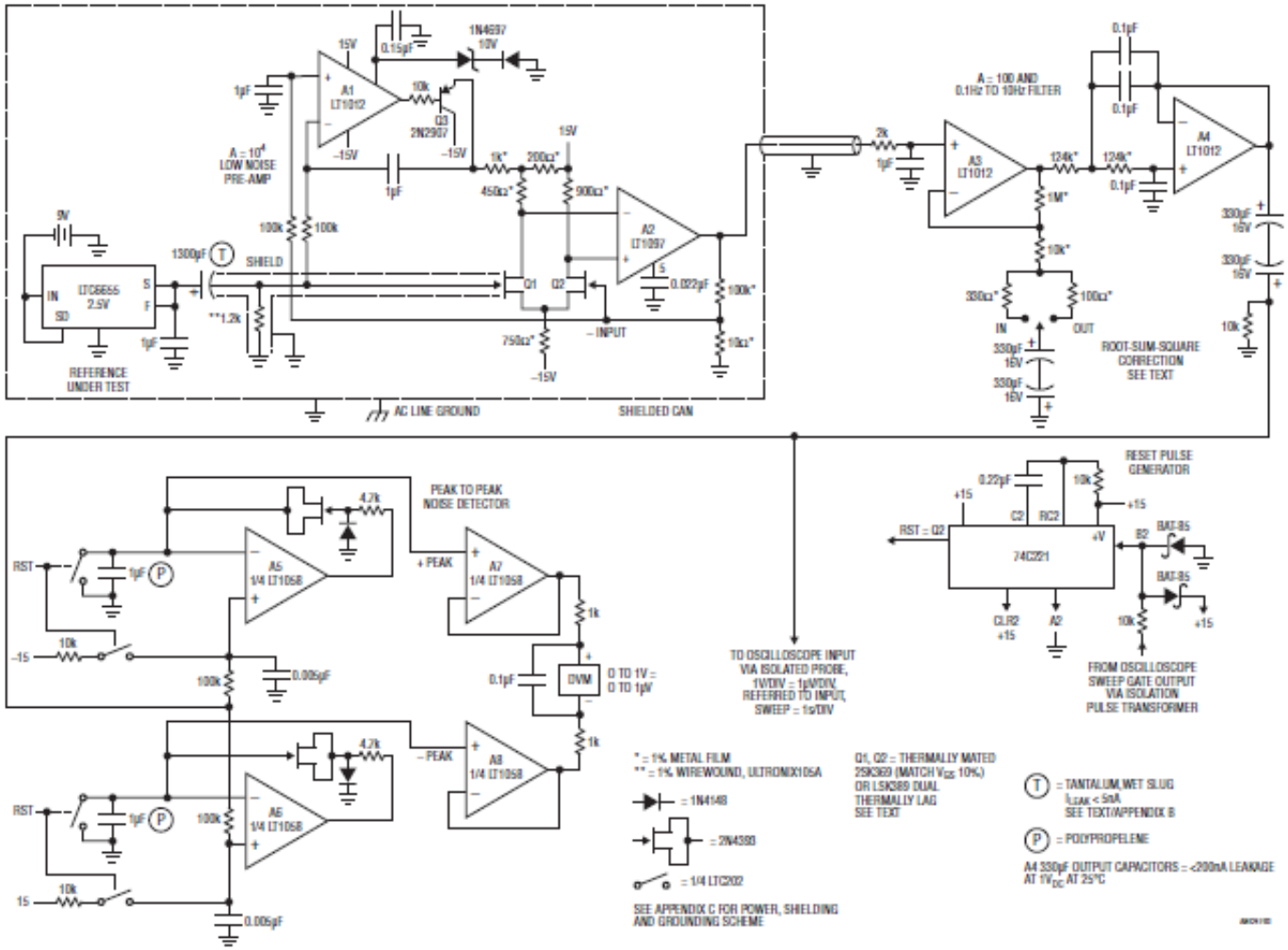



**Figure 3. Detailed Noise Test Circuitry. Thermally Lagged Q1-Q2 Low Noise J-FET Pair Is DC Stabilized by A1-Q3; A2 Delivers A = 10,000 Pre-Amplifier Output. A3-A4 form 0.1Hz to 10Hz ,A = 100, Bandpass Filter; Total Gain Referred to Pre-Amplifier Input Is $10^6$. Peak to Peak Noise Detector, Reset by Monitoring Oscilloscope Sweep Gate, Supplies DVM Output**



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# References

- Linear Technology
  - LT 6655 Data sheet
  - LT 1128 Data sheet
  - Application Note AN124
- Analog devices
  - AD9656 Data sheet
  - Application Note AN835 for ADC specification testing and performance evaluation

# Thanks